Amendments to the Specification

Please replace the paragraph beginning on page 5, line 6 with the following amended paragraph:

~~FIGURE~~ Figure 1A shows a semiconductor substrate over which a dielectric layer, a gate layer and dielectric film have been formed in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 5, line 10 with the following amended paragraph:

~~FIGURE~~ Figure 1B shows the structure of Figure 1A after that portion of the dielectric film that extends within the non-core region has been removed in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 5, line 14 with the following amended paragraph:

~~FIGURE~~ Figure 1C shows the structure of Figure 1B after an anti-reflective coating has been deposited so as to form a gate film stack that overlies a dielectric layer and that is thicker in the core region than in the non-core region in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 5, line 19 with the following amended paragraph:

~~FIGURE~~ Figure 1D shows the structure of Figure 1C after a photoresist mask has been formed thereover in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 6, line 5 with the following amended paragraph:

~~FIGURE~~ Figure 1F shows the structure of Figure 1E after a photoresist mask has been formed thereover in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 7, line 15 with the following amended paragraph:

~~FIGURE~~ Figure 3A shows a gate film stack that overlies a dielectric layer and that is thicker in the core region than in the non-core region, after a photoresist mask has been formed thereover, in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 8, line 1 with the following amended paragraph:

~~FIGURE~~ Figure 3C shows the structure of Figure 3B after a photoresist mask has been formed thereover in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 8, line 8 with the following amended paragraph:

~~FIGURE~~ Figure 3E shows the structure of Figure 3D after a photoresist mask has been formed thereover in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 9, line 14 with the following amended paragraph:

~~FIGURE~~ Figure 5A shows a dielectric layer and a gate film stack that are formed on a semiconductor substrate, and a dielectric mask that overlies the gate film stack in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 10, line 1 with the following amended paragraph:

~~FIGURE~~ Figure 5D shows the structure of Figure 5C after a photoresist mask has been formed thereover in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 10, line 5 with the following amended paragraph:

~~FIGURE~~ Figure 5E shows the structure of Figure 5D after an etch has been performed and after removal of the photoresist mask in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 10, line 9 with the following amended paragraph:

~~FIGURE~~ Figure 5F shows the structure of Figure 5E after a BARC layer has been deposited and after a photoresist mask has been formed in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 10, line 13 with the following amended paragraph:

~~FIGURE~~ Figure 5G shows the structure of Figure 5F after an etch has been performed and after removal of the remaining BARC layer and photoresist mask in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 10, line 17 with the following amended paragraph:

~~FIGURE~~ Figure 6A shows a dielectric layer and a gate film stack that are formed on a semiconductor substrate and a photoresist mask that overlies the gate film stack in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 11, line 1 with the following amended paragraph:

~~FIGURE~~ Figure 6C shows the structure of Figure 6B after a photoresist mask has been formed thereover in accordance with an embodiment of the present invention.

Please replace the paragraph beginning on page 12, line 16 with the following amended paragraph:

Figures ~~1A-6F~~ 1A-6D illustrate a method for forming self-aligned contact devices in a first region of a semiconductor substrate (core region) and non-self-aligned contact devices in a second region (non-core region) of the semiconductor substrate. The term "SAC devices" includes those types of semiconductor devices that use a self-aligned contact process for establishing a connection to gate structures and/or source and drain regions and includes semiconductor devices that include self-aligned contacts that couple to gate

structures and/or source and drain structures. The term "non-SAC devices" includes those types of semiconductor devices that do not use a self-aligned contact process for establishing a connection to gate structures and/or source and drain regions and includes semiconductor devices that do not include self-aligned contacts that couple to gate structures and/or source and drain structures.

Please replace the paragraph beginning on page 13, line 5 with the following amended paragraph:

As shown by Figures 1A-1C a dielectric layer 2 and a gate film stack 100 are formed over semiconductor substrate1. Semiconductor substrate 1 can be either N or P type and can include isolation regions (e.g., using shallow trench isolation processing steps) depending on the device requirements. Referring now to Figure 1A, a dielectric layer 2 is formed over substrate 1. In the present embodiment dielectric layer 2 is formed by depositing or growing a layer of dielectric material over semiconductor substrate 1 such that dielectric layer 2 directly overlies substrate 1. In the present embodiment dielectric layer 2 is a thin layer (e.g., 5 to 100 Angstroms) of silicon dioxide (SiO_2) or other type of ~~gate oxide~~ dielectric that extends within all of core region 20 and non-core region 30.

Please replace the paragraph beginning on page 18, line 12 with the following amended paragraph:

An etch is performed so as to remove those portions of gate layer 3 and ARC 5 that are not covered by mask 7, forming the structures shown in Figure 1G. In the present embodiment a fluorine based etch is used. In the present embodiment a fluorine based etch is used to pattern ARC 5 and a chlorine (CL_2)-hydrogen bromide (HBr)-based

etch is used to pattern gate layer 3.[[..]] The etch exposes portions of substrate 1 and defines gate structures 32 in non-core region 30. In addition, the etch forms portions of lines 21 within non-core region 30.

Please replace the paragraph beginning on page 19, line 7 with the following amended paragraph:

Mask 6 and mask 7 overlap where lines cross between core region 20 and non-core region 30. In the embodiment shown in Figure 2D, mask 7 defines line 21 by structure 21A in mask 7 and includes a broadened region 22 that has a "hammerhead" shape. Broadened region 22 is formed in mask 7 along each line ~~21A~~ 21a that extends between core region 20 and non-core region 30. Broadened region 22 extends within region 25 so as to form a broadened region 23 in each resulting line ~~21B~~ 21b, assuring good contact at the boundary, even when there is significant mask alignment error between the two masks in a direction perpendicular to line 21 as is illustrated in Figure 2E.

Please replace the paragraph beginning on page 20, line 9 with the following amended paragraph:

Referring now to Figure 3A, a mask 8 is formed that exposes portions of both core region 20 and non-core region 30. In the present embodiment mask 8 defines gate structures and defines lines within both core region 20 and non-core region 30. Mask 8 can be formed by depositing, exposing and developing a layer of photoresist so as to form a desired mask pattern. Because of the thickness differences between core region 20 and non-core region 30, in the present embodiment photolithography conditions are

carefully controlled to closely match the critical dimension and photo resist profile between core region 20 and non-core region 30.

Please replace the paragraph beginning on page 23, line 7 with the following amended paragraph:

Figures 4A-4E show how a line design 41, shown in Figure 4A can be implemented that extends between core region 20 and non-core region 30. In the present embodiment, mask 8 defines line 41 by structure [[41A]] 41a in mask 8 such that the etch shown in Figure 3B patterns ARC 5 (and underlying dielectric film 4), exposing portions of gate layer 3. As shown in Figure 4B mask 9 does not cover gap 26. This will cause the etch of core region 20 to also etch gap 26, forming the structure shown in Figure 4C. This exposes the underlying hardmask 4b and portions of the field oxide layer 40. Similarly, mask 10 does not cover a gap 27. Accordingly, portions of gaps 26-27 are etched during both etches. This double-etch prevents bridging of lines 41, even when there is significant mask misalignment. Line [[41A]] 41a is self-aligned as a result of the use of ARC 5 and dielectric film 4 to define line [[41A]] 41a. More particularly, misalignment between masks 9 and 10 will not alter the position of the line as its position is defined by the selective etch of ARC 5 and dielectric film 4.

Please replace the paragraph beginning on page 28, line 6 with the following amended paragraph:

Figures [[6A-6E]] 6A-6D illustrate a method for forming self-aligned contact devices in a core region and non-self-aligned contact devices in a non-core region of a semiconductor substrate in which dielectric layer 2 and gate film stack 200 are formed in the same manner as in the embodiment illustrated in Figure 5A. This forms a gate film stack 200

that includes gate layer 3 and dielectric film 4 having one or more layers of ARC 4a and one or more layers of hardmask 4b.